Boolean Differential Calculus Applied in Logic Testing

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Abstract: The advent of deep-submicron (DSM) designs has created new difficulties in clock skew and power delivery, while the latest nanometer technologies have demonstrated that defects are located predominantly in routing. Inductive fault analysis of actual circuits suggests that bridging faults account for thirty to fifty percent of all faults. Other studies also show that most silicon defects exhibit bridging fault behaviour and test strategies that use simple fault model, such as single stuck-at, do not satisfy the growing test quality requirements. Boolean differential calculus applied for such faults, used both for design and testability, is still a new and emerging area. Undetectable bridging faults belong to hard to detect faults class and can invalidate several sets of tests designed for classical stuck-at faults. This work is using Boolean differential calculus in order to obtain relations of internal chip lines for undetectable bridging faults..

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